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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,563	04/08/2004	Baki Acikel	22994-07841	2612
758 7590 02/20/2007 FENWICK & WEST LLP SILICON VALLEY CENTER 801 CALIFORNIA STREET MOUNTAIN VIEW, CA 94041			EXAMINER MALDONADO, JULIO J	
			ART UNIT 2823	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		02/20/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/822,563

Applicant(s)

ACIKEL ET AL.

Examiner

Julio J. Maldonado

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 November 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) 11, 12, 25 and 30 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10, 13-24, 26-28 and 31 is/are rejected.
- 7) ☒ Claim(s) 29 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 20061106.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

1. The addition of claim 31 as set forth in the response filed 11/29/2006 is acknowledged.
2. Claims 1-31 are pending in the application, wherein claims 11, 12, 25 and 30 were previously withdrawn.

Allowable Subject Matter

3. The indicated allowability of claim 21 is withdrawn in view of the newly discovered reference(s) to Hartner et al. (U.S. 6,503,792 B2). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakata (U.S. 2004/0087082 A1) in view of Olewine et al. (U.S. 2003/0067023 A1, hereinafter Olewine).

In reference to claim 1, Nakata (Figs.2A-2F) teaches a method of forming a MIM capacitor including the steps of forming a platinum bottom electrode (3) supported by a substrate (1), including forming a lateral shape of the bottom electrode; forming a silicon nitride thin film dielectric region (5) over the bottom electrode (3), including producing silicon nitride material over the bottom electrode (3) only after the lateral shape of the

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bottom electrode (3) is formed; and forming a top electrode (6) over the silicon nitride thin film dielectric region (5) (Nakata, [0018] – [0026]).

Nakata fails to disclose wherein the thin film dielectric region is made of BST. However, Olewine teaches a method of forming a MIM capacitors including forming a lower electrode, a thin film dielectric region and a top electrode, wherein said thin film dielectric region is made from a material selected from the group including silicon nitride, tantalum oxide and BST (Olewine, [0008]).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Nakata and Olewine to enable forming the thin film dielectric region of Nakata using the materials according to the teachings of Olewine because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of forming the disclosed thin film dielectric region of Nakata and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

In reference to claims 2, 4, 5 the combined teachings of Nakata and Olewine teach wherein the step of forming a bottom electrode supported by a substrate comprises forming a lift off mask over the substrate, the lift off mask defining the lateral shape of the bottom electrode; depositing a layer of bottom electrode material over the lift off mask; and removing the lift off mask, thereby forming the lateral shape of the bottom electrode (Nakata, [0018] – [0026]).

In reference to claims 3 and 6-8, the combined teachings of Nakata and Olewine et al. teach wherein the step of forming a lift off mask over the substrate comprises

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depositing a photoresist lift off mask over the substrate; and the step of depositing a layer of bottom electrode material over the lift off mask comprises depositing a platinum layer and a gold layer over the photoresist lift off mask (Nakata, [0018] – [0026]).

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakata ('082) in view of Olewine ('023) as applied to claims 1-8 above, and further in view of Nishioka et al. (U.S. 5,489,548, hereinafter Nishioka).

The combined teachings of Nakata and Olewine substantially teach all aspects of the invention but fail to disclose wherein the bottom electrode consists essentially of a conductive oxide. However, Nishioka teach a method of forming a high dielectric constant capacitor including forming a bottom electrode, a BST dielectric region, and a top electrode, wherein said electrode are made from a group of material including platinum, gold and conductive oxides (Nishioka, column 9, lines 7 – 23).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Nakata and Olewine with Nishioka to enable forming the bottom electrode of the combination of Nakata and Olewine using the materials according to the teachings of Nishioka because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of forming the disclosed bottom electrode of Nakata and Olewine and art recognized suitability for an intended purpose has been recognized to be motivation to combine.

MPEP 2144.07.

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7. Claims 10, 13, 14, 16-24, 26, 28 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakata ('082) in view of Hartner et al. (U.S. 6,503,792 B2, hereinafter Hartner).

In reference to claims 10, 13, 14, 16, 21, 22, 23, 26 and 31, Nakata (Figs.2A-2F) teaches a method of forming a MIM capacitor including the steps of forming a platinum bottom electrode (3) supported by a substrate (1), including forming a lateral shape of the bottom electrode; forming a silicon nitride thin film over the bottom electrode (3) and patterning said film to form a silicon nitride thin film dielectric region (5) over the bottom electrode (3), including producing silicon nitride material over the bottom electrode (3) only after the lateral shape of the bottom electrode (3) is formed; and forming a top electrode (6) made of platinum and gold over the silicon nitride thin film dielectric region (5) after forming said silicon nitride thin film dielectric region (5) (Nakata, [0018] – [0026]).

Nakata fails to disclose wherein the thin film dielectric region is made of BST, and forming said top electrode over the BST thin film immediately after forming said BST but before forming the BST lateral shape and annealing the BST thin film material. However, Hartner (Figs.2A-2C) teaches a method of forming BST parallel plate capacitor including the steps of forming a platinum bottom electrode (31) over a substrate (1); forming a BST thin film dielectric region over the bottom electrode including producing BST thin film material over the bottom electrode; forming a platinum layer over and subsequently after forming said BST layer; patterning said platinum layer to form a platinum top electrode; patterning said BST layer to form a BST thin film after

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patterning said platinum layer, wherein said patterning of the platinum layer and BST thin film material is performed by any conventional patterning process; and after forming said platinum top electrode and said BST thin film, annealing said BST thin film (Hartner, column 4, line 11 – column 5, line 51).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Nakata and Hartner to enable etching and patterning the top electrode and the BST thin film of Nakata according to the teachings of Hartner because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed patterning step of Nakata and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

It would also have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Nakata and Hartner to enable annealing the BST film to correct any crystalline damage done to the BST film after the patterning step (Hartner, column 5, lines 32 – 43).

In reference to claims 17-20 and 28, the combination of Nakata and Hartner teach forming a passivation structure over the BST thin film dielectric region, including producing passivation material over the BST material only after the top electrode material is produced over the BST material after the top electrode layer is formed and wherein said passivation is made of either silicon nitride (Nakata, [0026]) or silicon oxide (Hartner, column 4, lines 36 – 52).

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In reference to claim 24, the combined teachings of Nakata and Hartner teach forming the platinum bottom electrode using a lift off process (Nakata, [0022]).

8. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakata ('082) in view of Hartner ('792) as applied to claims 10, 13, 14, 16-24, 26, 28 and 31 above, and further in view of Moslehi (U.S. 5,273,609).

Still the combination of Nakata and Hartner fail to disclose wherein the step of forming a layer of top electrode material over the BST thin film material comprises depositing a platinum layer over the BST thin film material, wherein deposition of the platinum layer occurs in a same processing chamber as production of the BST thin film material, and without interim removal of the BST parallel plate capacitor from the processing chamber. However, Moslehi teaches a deposition process, wherein said process is performed in a multi-step processing system and wherein multiple thin layers can be deposited in situ (Moslehi, column 7, line 60 – column 8, line 9). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Nakata and Hartner with Moslehi to enable forming the layers of Nakata and Hartner in the processing system of Moslehi for the further advantage of reducing processing time (Moslehi, column 6, lines 36 – 47).

9. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakata ('082) in view of Hartner ('792) as applied to claims 10, 13, 14, 16-24, 26, 28 and 31 above, and further in view of Nishioka et al. (U.S. 5,489,548, hereinafter Nishioka).

The combined teachings of Nakata and Hartner substantially teach all aspects of the invention but fail to disclose wherein the bottom electrode consists essentially of a

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conductive oxide. However, Nishioka teach a method of forming a high dielectric constant capacitor including forming a bottom electrode, a BST dielectric region, and a top electrode, wherein said electrode are made from a group of material including platinum, gold and conductive oxides (Nishioka, column 9, lines 7 – 23).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Nakata and Hartner with Nishioka to enable forming the bottom electrode of the combination of Nakata and Hartner using the materials according to the teachings of Nishioka because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of forming the disclosed bottom electrode of Nakata and Hartner and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Response to Arguments

Applicant's arguments filed 11/29/2006 have been fully considered but they are not persuasive.

Applicants argue, "...All rejections rely on Nakata as the primary reference. However, it has not been established that Nakata qualifies as prior art. The current application claims priority under 35 U.S.C. § 120 to U.S. Patent Appl. No. 10/144,185 (the '185 application, currently issued as U.S. Patent No. 6,683,341), which has a filing date of May 10, 2002. Elected pending claims 1-10, 13-24, 26-29 and 31 are supported, for example, by FIGS. 4A-4C and the related text of the '185 application. Therefore, the current application is entitled to a filing date of May 10, 2002...". In response to this

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argument, Nakata was filed on Mar. 10, 2003, which is too late to qualify as prior art under 35 U.S.C. § 102(e). Accordingly, Applicants respectfully request that Nakata be withdrawn as prior art and that all elected pending claims 1-10, 13-24, 26-29 and 31 as amended be allowed on this basis...". In response to this argument, the Nakata reference is a division of another earlier application filed 11/21/2001 and thus Nakata qualifies as prior art.

Allowable Subject Matter

Claim 29 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record teaches away from annealing the BST thin film dielectric region only after forming the passivation structure as disclosed in claim 29.


Conclusion

Applicants are encouraged, where appropriate, to check Patent Application Information Retrieval (PAIR) (<http://portal.uspto.gov/external/portal/pair>) which provides applicants direct secure access to their own patent application status information, as well as to general patent information publicly available.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax number for this group is 571-273-8300. Updates can be found at <http://www.uspto.gov/web/info/2800.htm>.


Julio J. Maldonado
February 7, 2007

Julio J. Maldonado
Patent Examiner
Art Unit 2823



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